REMARKS

The Office Action of 1/19/2006 rejected claims 1-18 under 35 U.S.C. 112, second paragraph, as indefinite. I assume the Examiner meant claims 1 and 10, not 18.

The Examiner cited the phrase "unequal logic signal currents" as being misdescriptive. The phrase is amended herein omitting the word "logic" and adding a definition phrase at the end of claims 1 and 10. It is a fair reading of the application that the logic states are defined by which of the conductors has the larger current. See original application page 4, lines 5-6, where it reads, "The unequal current sources are switch between the two transmission lines in response to a logic signal." That is a input logic signal switches the higher current to the conductor that has the lower current and visa-versa. That defines "logic' states. Also, see page 5, lines 21-25, where it read (referring to FIG. 4A) , "In one logic state Ia is a positive current out into the first transmission line 50 and Ib is a negative current in from a second transmission line 52. In the opposite logic state Ia is a negative current from the first transmission line 50 and Ib is a positive current into the second transmission line 52. In another preferred embodiment it is possible to have no current into either transmission line."

So the logic states are by switching or reversing the polarity of the current into the two conductors, or the to have one logic state defined by the unequal current into the two conductors and the other state being with no current.

As used in the original application it is very clear that the currents are reversed and that reversal defines two logic states. I trust the Examiner will agree. I would appreciate, if an error or confusion remains, that the Examiner call me at my direct number below, as I feel that the logic states are well defined in the original application.

On page 3 of the Office Action, the Examiner rejected clams 1-2, 6-7, 9-12, 15-16 and 18 under 35 U.S.C. 102(b) as being anticipated by Van Brunt et al. (USP 5,592,510), hereafter '510. Note the '510 patent is directed to minimizing common mode issues, while the present invention specifically disclaims the need for any such circuitry, as detailed below.

Applicant's attorney would like to point out an existing limitation in claims 1 and 10. That limitation is:

> a terminating resistor connected between the distal ends of the first and the second signal carrying conductors, ***wherein no common mode signals are introduced into or measured along the terminating resistor,***

Emphasis added here to highlight that limitation that no common mode signals are introduced at the transmission line terminating resistor. Please refer to the original application, page 6, lines 25-30. Here the application specifically disclaims any need for compensation for common mode signals. No common mode circuitry can be introduced at the terminating resistor with the claims as now presented. Note, that the entire unequal current analysis in the present invention would be changed, compromised and/or harmed by any common mode signals as suggested by the '510 patent.

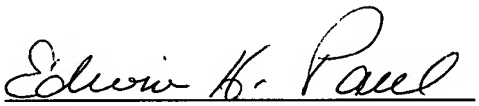
It is respectfully pointed out that the '510 reference was distinguished in the March 22, 2005 response to an Office Action of 12/22/2004. Also Mitsuo (JP 07-307661) was brought up in the 12/22/2004 action and distinguished in the March 22, 2005 response.

Neither the '510 nor Mitsuo were brought up the subsequent Office Action of 5/03/2005.

Claims 1-18 as now presented distinguish the cited prior art and a Notice of Allowance is respectfully requested.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



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